

Remarks

Claims 1-17, 21, and 23-25 are pending. Reconsideration of claims 1-17, 21, and 23-25 is requested.

Claims 1, 3-6, 12-14, 17, 21, and 23 stand rejected under 35 U.S.C. §102(b) as being anticipated by Shue et al. (U.S. Patent No. 5,970,378, hereafter "Shue"). The Examiner has asserted that Shue discloses each of the elements and limitations contained in claims 1, 3-6, 12-14, 17, 21, and 23. For example, the Examiner has asserted that Shue teaches a process whereby a glue layer is treated to improve the adhesiveness characteristics of the glue layer, as generally recited in independent claims 1, 12, and 21. However, contrary to the conclusions of the Examiner, Shue does not teach application of an inter-treatment process to improve the adhesiveness of a glue layer together with the other limitations of the claims.

Shue discloses "a method for forming a titanium nitride layer within an integrated circuit." Abstract. Shue further discloses that titanium nitride layers are commonly used in integrated circuit fabrication "as either adhesion promoter layers or barrier layers." Col. 1, lns. 23-24. Shue teaches the performance of various processing steps on a titanium nitride layer; however, as will be shown, the processing steps do not improve the adhesion qualities of the titanium nitride layer.

Specifically, Shue describes the formation of a virgin titanium nitride layer on a series of patterned planarized pre-metal dielectric layers through chemical vapor deposition. See col. 5, lns. 10-50; Fig 2. The virgin titanium nitride layer is then refined using plasma to form a refined titanium nitride layer. See col. 6, lns. 9-36; Fig. 3. The refined titanium nitride layer is then subjected to another plasma exposure containing nitrogen without hydrogen to form a densified titanium nitride layer. See col. 6, lns. 37-45. "Through treatment of the refined titanium nitride layer 22' with the second plasma 26 to form the densified titanium nitride layer 22" there is formed a densified titanium nitride layer 22" exhibiting a low resistivity as evidenced by a reduced sheet resistance" in Fig. 4. Col. 6, lns. 46-50, emphasis added. In addition to improving the resistivity of the titanium nitride layer, the processing steps provide a titanium nitride layer

with superior step coverage and low impurities concentration. See Abstract. In other words, Shue discloses the use of an adhesion promoting layer and further discloses processing steps being performed on the adhesion layer; however, Shue does not teach or suggest that the processing steps improve the adhesiveness of the adhesion promoting layer. The improvements in the adhesion promoting layer include improved step coverage, low resistivity, and low impurities concentration, but Shue does not teach or suggest that improved adhesion is an additional benefit by the described processing steps.

In contrast, claim 1 calls for “performing an inter-treatment on the glue layer, wherein the inter-treatment affects the upper and lower surfaces of the glue layer and improves an adhesive interface between the glue layer and the first layer.” Claim 12 calls for “applying the selected treatment process to affect the upper and lower surfaces of the glue layer” and “wherein the treatment process enhances an adhesiveness between the dielectric layer and the metal layer.” Claim 21 calls for “performing an inter-treatment on the glue layer to alter upper and lower surfaces of the glue layer for improved adhesiveness.”

Accordingly, claims 1, 12, and 21 are believed to be patentably distinct from that disclosed and/or suggested by Shue. Claims 1-11, 13-17, and 23-24 depend from and further limit claims 1, 12, and 21, respectively, and, as such, are believed to also be in condition for allowance.

Claims 21, 23, and 25 stand rejected under 35 U.S.C. §102(b) as being anticipated by Dixit et al. (U.S. Patent No. 6,355,558, hereafter “Dixit”). Dixit discloses “[a] metallization structure, and associated method, for filling contact and via apertures to significantly reduce the occurrence of microvoids and provide desirable grain orientation and texture.” Abstract. Like Shue, Dixit fails to teach or suggest processing or treatment steps to improve the adhesion characteristics of a glue or adhesion layer, together with the other limitations of the claims.

Dixit et al. discloses that “an optional barrier fortification step [is] performed to ‘stuff’ the barrier layer to improve the performance of the barrier layer to keep the subsequently deposited Al from diffusing, or spiking, through the barrier layer into the underlying silicon.” Col. 4, lns.

52-56. Thus, Dixit teaches a step for improving the blocking performance of the barrier layer – not for improving any adhesiveness of the layer. In this regard, Dixit et al. fails to teach or suggest “a method for improving an interface in a semiconductor device” that includes “performing an inter-treatment on the glue layer to alter upper and lower surfaces of the glue layer for improved adhesiveness,” as called for in claims 21, 23, and 25.

Accordingly, claims 21, 23, and 25 are believed to be patentably distinct from that disclosed and/or suggested by Shue. Allowance thereof is therefore requested.

Regarding the rejections of claims 2, 7-11, 15-16, and 24 Applicant respectfully disagrees with the Examiner with respect to the art as applied, but in light of claims 2, 7-11, 15-16, and 24 depending from what are believed otherwise allowable claims, Applicant does not believe that additional remarks are necessary and requests allowance of claims 2, 7-11, 15-16, and 24 at least pursuant to the chain of dependency.

Therefore, it is clear from at least the foregoing that independent claims 1, 12, 21, and 25 are patentably distinct from that disclosed by the art of record and, therefore, are in condition for allowance. Dependent claims 2-11, 13-17, 23, and 24 depend from and further limit independent claims 1, 12, and 21 and therefore are allowable as well.

As no outstanding issues remain, an early formal notice of allowance of claims 1-17, 21, and 23-25 is requested.

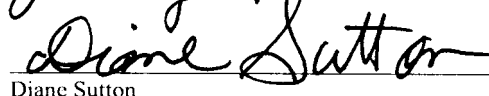
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I hereby certify that this correspondence is being filed with the U.S. Patent and Trademark Office via EFS-Web on January 22, 2007.


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